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WENDEROTH, LIND & PONACK, L.L.P.
2033 K STREET N. W.
SUITE 800
WASHINGTON, DC 20006-1021

EXAMINER	
PHAN, THIEM D	

ART UNIT	PAPER NUMBER
3729	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/538,506	MURAKAMI, KEIICHI	
	Examiner	Art Unit	
	THIEM PHAN	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/04/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 6/04/08 has been fully considered and made of record.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yasue et al (US 6,010,768).

Regarding claim 1, Yasue et al teach a method of producing multilayer printed circuit board, comprising the steps of:

- obtaining a printed wiring board (Fig. 3B, 1) with a circuit pattern (Fig. 3B, 5 & 5') formed on a surface of the printed wiring board;
- forming a resin layer (Fig. 3C, 14) by superposing a semi-cured resin sheet on the surface of the printed wiring board containing said circuit patterns;
- pressing and forcing the resin layer into spaces between said circuit patterns (Fig. 3C, 5; col. 23, lines 56-58);
- curing said resin layer (Col. 23, lines 52 & 53); and
- polishing said cured resin layer, thereby exposing said circuit patterns (Col. 24, lines 1-4); except for having the complementary resin circuit patterns complementary to said circuit patterns formed on the semi-cured resin sheet and facing said circuit patterns.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to have the complementary resin circuit patterns complementary to said circuit patterns formed on the semi-cured resin sheet and facing said circuit patterns because applicant has not disclose that having the complementary resin circuit patterns complementary to said circuit patterns formed on the semi-cured resin sheet and facing said circuit patterns provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected applicant's invention to perform equally well with a resin layer (Fig. 3C, 14) on the printed wiring board because it fills spaces between circuit patterns (Fig. 3C, 5) as well.

Therefore, it would have been an obvious matter of design choice to modify Yasue et al to obtain the invention as specified in Claim 1 as well.

4. Claims 3, 4 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasue et al in view of Applicant's Admitted Prior Art, hereinafter AAPA.

Regarding claims 3 and 20, Yasue et al teach a method of producing multilayer printed circuit board, which reads on applicant's claimed invention; except for pressing the resin layer against the printed circuit board at reduced pressure atmosphere.

AAPA teaches a method of manufacturing multilayer printed wiring board, which teaches the pressing of the resin sheet in a reduced pressure atmosphere via a smooth plate (Specification, page 1, section 0003) against the circuit patterns formed by subtractive method (Specification, page 1, section 0002), in order to flatten the printed circuit board.

It would be obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Yasue et al by applying the resin sheet pressing at reduced pressure atmosphere, as taught by AAPA, in order to flatten the printed circuit board.

Regarding claim 4, Yasue et al in view of AAPA teach a method of producing multilayer printed circuit board including the pressing of resin layer with a smooth plate (AAPA, page 1, section 0003) and the resin particles of size about $1/10^{th}$ of the circuit patterns thickness (Yasue et al; col. 23, lines 42-45), which reads on applicant's claimed invention; except for pressing the resin layer with a metallic foil having a roughened surface facing said resin layer.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to have a metallic foil with a roughened surface pressing against said resin layer because applicant has not disclose that having a metallic foil with a roughened surface pressing against said resin layer provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected applicant's invention to perform equally well with a smooth foil pressing against the resin layer because it forces the resin layer to fill spaces between circuit patterns (AAPA, page 1, section 3; Yasue et al, fig. 3C, 5) as well.

Therefore, it would have been an obvious matter of design choice to modify Yasue et al in view of AAPA to obtain the invention as specified in Claim 4.

5. Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasue et al in view of AAPA and further view of Fukutomi et al (US 6,268,648).

Regarding claims 5 and 6, Yasue et al in view of AAPA teach a method of producing multilayer printed circuit board including the copper circuit patterns (AAPA, page 1, section 0002) and the pressing plate (AAPA, page 1, section 0003), which reads on applicant's claimed invention; except for having the pressing metallic foil or plate formed of nickel.

Fukutomi et al teach a method of manufacturing a semiconductor chip package substrate, using a nickel metallic layer (Fig. 7, 11) is used to press and bury the copper wiring (Fig. 7, 12) against and into the prepreg (Fig. 7, 14) in order to form a barrier layer (Abstract) to a carrier layer (Fig. 7, 10).

It would be obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Yasue et al in view of AAPA by applying the nickel metallic layer, as taught by Fukutomi et al, in order to form a barrier layer to a carrier layer.

Regarding claims 7 and 8, Yasue et al semi-cured resin sheets are formed from a thermosetting epoxy resin or thermosetting resin (Col. 7, lines 32-37).

Response to Arguments

6. Applicants' arguments filed 06/04/08 have been fully considered but they are not persuasive for the following reasons:

Applicants urge (Remarks, pages 5-7) that the prior art Yasue et al do not teach nor suggest "the complementary resin circuit patterns complementary to the circuit patterns" and this limitation is not a design choice because the benefit is disclosed in the specification and being further shown as evidence with respect to *In re Chu,* 66 F.3d 292, 36 USPQ2d 1089 (Fed. Cir. 1995).

First of all, in response to applicants' arguments, the prior art Yasue et al do suggest in an obviousness reasoning that the complementary resin circuit patterns (Fig. 3C to 3D, 14) are complementary to the circuit patterns (Fig. 3D, 5). Therefore, Yasue et al at a minimum teach the claimed limitation.

Second, applicants assert that there is technical advantage, as disclosed in the specification, to obtain a uniform resin layer through dense or sparse circuit patterns (Remarks, page 7). The examiner would like to ask and understand why and how there is such an advantage because the specification cites the words "technical advantages and benefits" and that doesn't automatically guarantee that there is a technical advantage but it is rather a disadvantage as explained below:

The resin paste itself is made of microsize particles (Yasue et al; col. 23, line 43) while the PCB circuit pattern is spaced at least in the millimeter width, a thousandth time bigger than the resin particles, which should not have any problem filling up any space between the circuit pattern, especially when being subjected to heat and pressure that create a layer thickness of resin and circuit pattern, and that layer thickness rather depends on the circuit pattern thickness itself than the resin particles. Furthermore, the circuit pattern is subjected to polishing effect to remove any trace of resin particles on some circuit pattern, this proves to be caused by the discrepancy in some of the circuit pattern thickness itself that leaves some resin particles on some thinner circuit pattern after the pressuring effect. Therefore, the limitation of providing a complementary resin circuit pattern before the heat and pressure effect proves to be unnecessary, to add costs to manufacturing process and finally a technical disadvantage in the claimed technical process.

Third, applicants cite the *In re Chu* (Remarks, page 7), and that case is also cited in MPEP 716.02(f), which sets forth a real advantage in the invention such as *In re Chu* where there is "an advantage of placement of a selective catalytic reduction catalyst in the bag retainer of an apparatus for controlling emissions". Therefore, it is improper to cite *In re Chu* in this case because there is no technical advantage and the limitation of a complementary resin circuit pattern before the heat and pressure effect is counter-productive in the totality of the claimed manufacturing method on record, because of the extra and unnecessary parts and labor involved for that complementary resin circuit pattern.

Regarding claims 3-8 and 20, they stand rejected as above (Sections 4 & 5) and with respect to the responses above.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure.

THIS ACTION IS MADE FINAL. Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim Phan whose telephone number is 571-272-4568. The examiner can normally be reached on M & Tu, 6AM - 2PM, and W & Th, 9AM – 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Vo can be reached on 571-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Phan Thiem/
Examiner, Art Unit 3729

September 3, 2008